AMENDMENTS

In the Claims:

1. (Currently Amended) A DLL circuit ~~having~~ comprising:

a first signal generator configured to set a first signal during a clock cycle of an internal clock during an initialization mode at a start of a burst;

a dummy delay circuit configured to generate a dummy delay corresponding to a delay between [[an]] the internal clock ~~delay~~ and an external clock[[,]];

~~a variable delay addition circuit having a coarse delay circuit and a fine delay circuit for adjusting delay amount according to a delay amount adjustment signal, and~~ a phase comparison circuit ~~for comparing~~ configured to compare a phase of the internal clock with a phase of a delay clock ~~input via the variable delay addition circuit and the dummy delay and outputting the~~ and output a delay amount adjustment signal; ~~to the variable delay addition circuit, the DLL circuit comprising:~~

a variable delay addition circuit comprising a coarse delay circuit and a fine delay circuit, the variable delay addition circuit adjusting a delay amount according to the delay amount adjustment signal to generate the delay clock during the initialization mode, the variable delay addition circuit being configured to receive the first signal, detect a duration time of the first signal until the end of the clock cycle of the internal clock, and set an initial value of the delay amount based on the duration time of the logic "1" of the first signal; and

~~a means for inputting a first signal set at a logic "1" during 1 clock cycle of the internal clock to the variable delay addition circuit via the dummy delay as an initialization mode at a start of burst;~~

~~a means for detecting duration time of the logic "1" of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit by setting the~~

~~delay amount of the coarse delay circuit in the variable delay addition circuit based on the duration time as the initialization mode at the start of burst; and~~

a clock ~~output means for generating~~ driver configured to generate an output clock that synchronizes with the external clock one clock cycle behind with the internal clock delayed by the ~~coarse delay circuit and the fine delay circuit in the variable delay addition circuit and with the~~ delay amount ~~of the coarse delay circuit and the fine delay circuit in the variable delay addition circuit~~ corrected according to the delay amount adjustment signal ~~output from the phase comparison circuit as~~ during a lock mode after initial setting of the delay amount during the initialization mode ~~in the variable delay addition circuit~~.

2. (Currently Amended) A DLL circuit ~~having~~ comprising:

a first signal generator configured to set a first signal during a clock cycle of an internal clock during an initialization mode at a start of a burst;

a dummy delay circuit configured to generate a dummy delay corresponding to a delay between [[an]] the internal clock ~~delay~~ and an external clock[[,]];

~~a variable delay addition circuit having a coarse delay circuit and a fine delay circuit for adjusting delay amount according to a delay amount adjustment signal, and~~ a phase comparison circuit ~~for comparing~~ configured to compare a phase of the internal clock with a phase of a delay clock ~~input via the variable delay addition circuit and the dummy delay and outputting the~~ and output a delay amount adjustment signal; ~~to the variable delay addition circuit, the DLL circuit comprising:~~

a variable delay addition circuit comprising a coarse delay circuit and a fine delay circuit, the variable delay addition circuit adjusting a delay amount according to the delay amount adjustment signal to generate the delay clock during the initialization mode, the variable delay addition circuit being configured to receive the first signal, detect a duration time of the first signal

until the end of the clock cycle of the internal clock, and set an initial value of the delay amount based on the duration time of the logic "1" of the first signal; and

~~a means for inputting a first signal set at a logic "1" during 1 clock cycle of the internal clock to the variable delay addition circuit via the dummy delay as an initialization mode at a start of burst;~~

~~a means for detecting duration time of the logic "1" of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit by setting the delay amount of the coarse delay circuit in the variable delay addition circuit based on the duration time as the initialization mode at the start of burst; and~~

a clock ~~output means for generating~~ driver configured to generate an output clock that synchronizes with the external clock one clock cycle behind with the internal clock delayed by the ~~coarse delay circuit and the fine delay circuit in the variable delay addition circuit and with the~~ delay amount ~~of the coarse delay circuit and the fine delay circuit in the variable delay addition circuit~~ corrected according to the delay amount adjustment signal ~~output from the phase comparison circuit as~~ during a lock mode after initial setting of the delay amount during the initialization mode ~~in the variable delay addition circuit~~,

wherein the coarse delay circuit ~~operates as the variable delay addition circuit and a means for storing~~ is configured to store setting of the initial value in the initialization mode and ~~operates~~ operate as a coarse variable delay addition circuit having coarse unit delay amount in the lock mode, and the fine delay circuit ~~operates~~ is configured to operate as a fine variable delay addition circuit adding delay amount for complementing the unit delay amount of the coarse delay circuit by having fine unit delay amount in the lock mode.

3. (Currently Amended) The DLL circuit according to claims 1 or 2 comprising a ~~means for preventing delay~~ delay preventing circuit configured to prevent delay from being added to the delay clock in the fine delay circuit ~~in the variable delay circuit,~~ when the phase of the delay clock obtained by adding predetermined threshold delay amount to the internal clock lags behind the internal clock, as a determination result of the phase comparison circuit in the lock mode.

4. (Currently Amended) The DLL circuit according to claims 1 or 2, wherein a delay element in the coarse delay circuit and the fine delay circuit ~~which form the variable delay addition circuit is formed of~~ comprises an inverter circuit and a circuit having inverse characteristics to the inverter circuit in terms of power supply voltage.

5. (Original) A variable delay addition circuit forming a DLL circuit having a dummy delay corresponding to delay between an internal clock delay and an external clock, a variable delay addition circuit including a coarse delay circuit and a fine delay circuit, for adjusting delay amount according to a delay amount adjustment signal, and a phase comparison circuit for comparing a phase of the internal clock with a phase of a delay clock input via the variable delay addition circuit and the dummy delay, outputting the delay amount adjustment signal to the variable delay addition circuit, and having a logic circuit for detecting that the delay amount of the coarse delay circuit and the fine delay circuit is set to be minimum by the delay amount setting signal output from the coarse delay circuit and the fine delay circuit, wherein the fine delay circuit includes a register that stores a signal output from the phase comparison circuit for bypassing the fine delay circuit, and a switching means for bypassing the delay addition unit in the fine delay circuit in response to the output of the register, and the delay addition unit in the fine delay circuit is bypassed and the delay is prevented from being added in the fine delay circuit, when the delay amounts of both the coarse delay circuit

and the fine delay circuit are set to be minimum and the phase of the delay clock lags behind the internal clock.

6. (New) A variable delay addition circuit implemented in a DLL circuit comprising a dummy delay circuit configured to generate a dummy delay corresponding to a delay between an internal clock delay and an external clock, and a phase comparison circuit configured to compare a phase of the internal clock with a phase of a delay clock and output the delay amount adjustment signal, the variable delay addition circuit being configured to adjust delay time according to the delay amount adjustment signal, the variable delay addition circuit comprising:

a coarse delay circuit; and

a fine delay circuit including a delay addition unit, a register configured to store a signal output from the phase comparison circuit for bypassing the fine delay circuit, and a switch for bypassing a delay addition unit in the fine delay circuit in response to the output of the register,

wherein the phase comparison circuit includes a logic circuit configured to detect when a delay amount of the coarse delay circuit and the fine delay circuit is set to be minimum via a delay amount setting signal output from the coarse delay circuit and the fine delay circuit, wherein the delay addition unit is bypassed and the delay is prevented from being added in the fine delay circuit when the delay amounts of both the coarse delay circuit and the fine delay circuit are set to be minimum and the phase of the delay clock lags behind the internal clock.